

# LOW POWER PROGRAMMABLE OSCILLATOR

## SERIES „LPOP“ 115.0—137.0 MHz

### FEATURES

- + High Frequency Programmable Low Power Oscillator for Low Cost
- + Excellent long time reliability
- + Excellent total frequency stability as low as  $\pm 20$  ppm over  $-40/+85^{\circ}\text{C}$
- + Excellent long term aging
- + Low power consumption of 4.8 mA typical
- + Programmable drive strength for improved jitter, system EMI reduction, or driving large capacitive loads
- + LVCMOS/HCMOS compatible output
- + Industry-standard packages: 2.0x1.6; 2.5x2.0; 3.2x2.5; 5.0x3.2; 7.0x5.0
- + Express samples within 1 day ex works
- + Pb-free, RoHS and REACH compliant / MSL1@260°C

### APPLICATIONS

- + Ideal for GPON/GPON, network switches, routers, servers, embedded systems, Telecom, Medical, Industrial, Consumer, etc.
- + Ideal for Ethernet, PCI-E, DDR, USB, SATA, Storage server, etc.

### GENERAL DATA<sup>[1]</sup>

PARAMETER AND CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
<b>FREQUENCY RANGE</b>						
Output Frequency Range	f	115	–	137	MHz	
<b>FREQUENCY STABILITY AND AGING</b>						
Frequency Stability	F_stab	-20	–	+20	PPM	Inclusive of initial tolerance at 25°C, 1st year aging at 25°C, and variations over operating temperature, rated power supply voltage and load.
		-25	–	+25	PPM	
		-50	–	+50	PPM	
<b>OPERATING TEMPERATURE RANGE</b>						
Operating Temperature Range	T_use	-20	–	+70	°C	Extended Commercial
		-40	–	+85	°C	Industrial
Storage Temperature Range	T_stor	-55	–	+125	°C	Storage
<b>SUPPLY VOLTAGE AND CURRENT CONSUMPTION</b>						
Supply Voltage	V <sub>DD</sub>	1.62	1.8	1.98	V	Contact Petermann-Technik for 1.5V support
		2.25	2.5	2.75	V	
		2.52	2.8	3.08	V	
		2.7	3.0	3.3	V	
		2.97	3.3	3.63	V	
		2.25	–	3.63	V	
Current Consumption	I <sub>DD</sub>	–	6.2	7.5	mA	No load condition, f = 125 MHz, V <sub>DD</sub> = 2.8V, 3.0V, 3.3V, or 2.25V to 3.63V
		–	5.4	6.4	mA	No load condition, f = 125 MHz, V <sub>DD</sub> = 2.5V
		–	4.8	5.6	mA	No load condition, f = 125 MHz, V <sub>DD</sub> = 1.8V
OE Disable Current	I_OD	–	–	4	mA	V <sub>DD</sub> = 2.5V to 3.3V, OE = GND, output is pulled down
		–	–	3.8	mA	V <sub>DD</sub> = 1.8V, OE = GND, output is pulled down
Standby Current	I_std	–	2.6	4.3	µA	ST = GND, V <sub>DD</sub> = 2.8V to 3.3V, output is pulled down
		–	1.4	2.5	µA	ST = GND, V <sub>DD</sub> = 2.5V, output is pulled down
		–	0.6	1.3	µA	ST = GND, V <sub>DD</sub> = 1.8V, output is pulled down

Note: 1. All electrical specifications in the above table are specified with 15 pF output load at default drive strength and for all V<sub>DD</sub>(s) unless otherwise stated.

## GENERAL DATA<sup>[1]</sup> (continued)

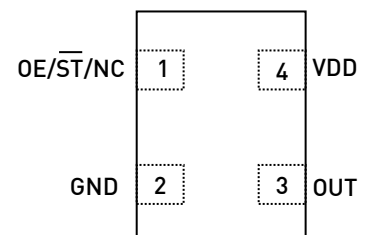
PARAMETER AND CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT	Condition
<b>LVC MOS OUTPUT CHARACTERISTICS</b>						
Duty Cycle	DC	45	–	55	%	All V <sub>DD</sub> s
Rise/Fall Time	Tr, Tf	–	1	2	ns	V <sub>DD</sub> = 2.5V, 2.8V, 3.0V or 3.3V, 20% - 80%
		–	1.3	2.5	ns	V <sub>DD</sub> = 1.8V, 20% - 80%
		–	0.8	2	ns	V <sub>DD</sub> = 2.25V - 3.63V, 20% - 80%
Output High Voltage	VOH	90%	–	–	V <sub>DD</sub>	IOH = -4 mA (V <sub>DD</sub> = 3.0V or 3.3V)
Output Low Voltage	VOL	–	–	10%	V <sub>DD</sub>	IOL = 4 mA (V <sub>DD</sub> = 3.0V or 3.3V)
<b>INPUT CHARACTERISTICS</b>						
Input High Voltage	VIH	70%	–	–	V <sub>DD</sub>	Pin 1, OE or ST
Input Low Voltage	VIL	–	–	30%	V <sub>DD</sub>	Pin 1, OE or ST
Input Pull-up Impedance	Z <sub>in</sub>	–	87	100	kΩ	Pin 1, OE logic high or logic low, or ST logic high
		2	–	–	MΩ	Pin 1, ST logic low
<b>STARTUP AND RESUME TIMING</b>						
Startup Time	T <sub>start</sub>	–	–	5	ms	Measured from the time V <sub>DD</sub> reaches its rated minimum value
Enable/Disable Time	T <sub>oe</sub>	–	–	130	ns	f = 115 MHz. For other frequencies, T <sub>oe</sub> = 100 ns + 3* cycles
Resume Time	T <sub>resume</sub>	–	–	5	ms	Measured from the time ST pin crosses 50% threshold
<b>JITTER</b>						
RMS Period Jitter	T <sub>jitt</sub>	–	1.93	3	ps	f = 125 MHz, V <sub>DD</sub> = 2.5V, 2.8V, 3.0V or 3.3V
		–	1.64	4	ps	f = 125 MHz, V <sub>DD</sub> = 1.8V
RMS Phase Jitter (random)	T <sub>phj</sub>	–	0.5	0.9	ps	Integration bandwidth = 900 kHz to 7.5 MHz
		–	1.3	2	ps	Integration bandwidth = 12 kHz to 20 MHz
<b>EXCELLENT RELIABILITY DATA</b>						
MTBF						500 million hours
Shock Resistance:						10.000 g
Vibration Resistance:						70 g

Note: 1. All electrical specifications in the above table are specified with 15 pF output load and for all V<sub>DD</sub>(s) unless otherwise stated.

## PIN DESCRIPTION

PIN	SYMBOL	FUNCTIONALITY
1	OE/ST/NC	Output Enable H or Open <sup>[2]</sup> : specified frequency output L: output is high impedance. Only output driver is disabled.
		Standby H or Open <sup>[2]</sup> : specified frequency output L: output is low (weak pull down). Device goes to sleep mode. Supply current reduces to I <sub>std</sub> .
		No Connect Any voltage between 0 and V <sub>DD</sub> or Open <sup>[2]</sup> : Specified frequency output. Pin 1 has no function.
2	GND	Power Electrically ground <sup>[3]</sup>
3	OUT	Output Oscillator output
4	V <sub>DD</sub>	Power Power supply voltage <sup>[3]</sup>

## TOP VIEW



Note: 2. In OE or ST mode, a pull-up resistor of 10kΩ or less is recommended if pin 1 is not externally driven. If pin 1 needs to be left floating, use the NC option.

3. A capacitor value of 0.1 μF between V<sub>DD</sub> and GND is recommended.

## TEST CIRCUIT AND WAVEFORM

FIGURE 1. TEST CIRCUIT

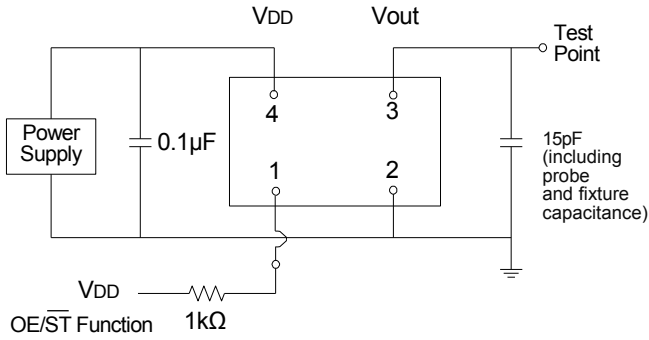
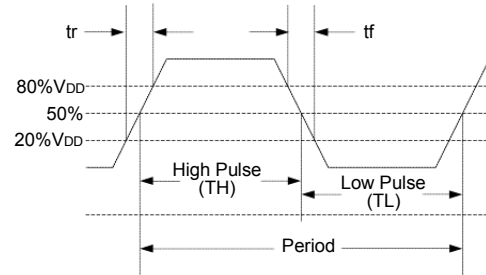


FIGURE 2. WAVEFORM



## TIMING DIAGRAMS<sup>(4)</sup>

FIGURE 3. STARTUP TIMING (OE/ST MODE)

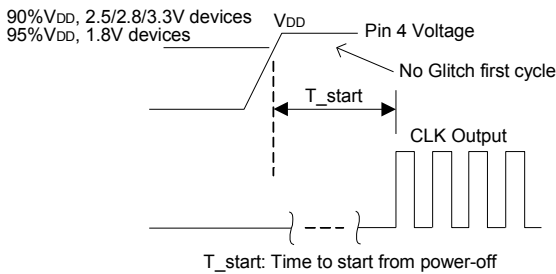


FIGURE 4. STANDBY RESUME TIMING (ST MODE ONLY)

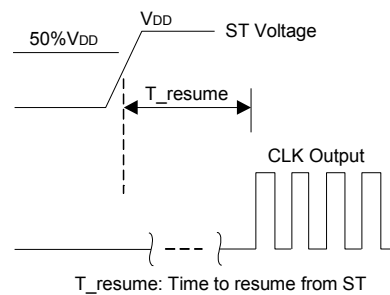


FIGURE 5. OE ENABLE TIMING (OE MODE ONLY)

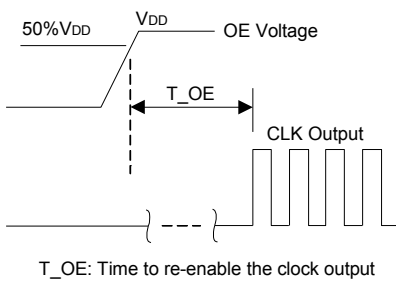
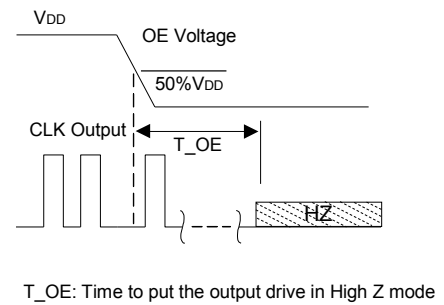


FIGURE 6. OE DISABLE TIMING (OE MODE ONLY)



Note: 4. LPOP supports no runt pulses and no glitches during startup or resume.

## PERFORMANCE PLOTS<sup>[5]</sup>

FIGURE 7. IDD vs. FREQUENCY

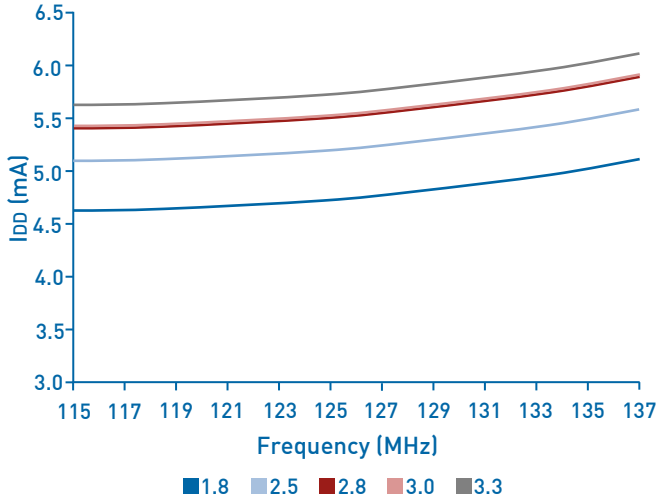


FIGURE 8. RMS PERIOD JITTER vs. FREQUENCY

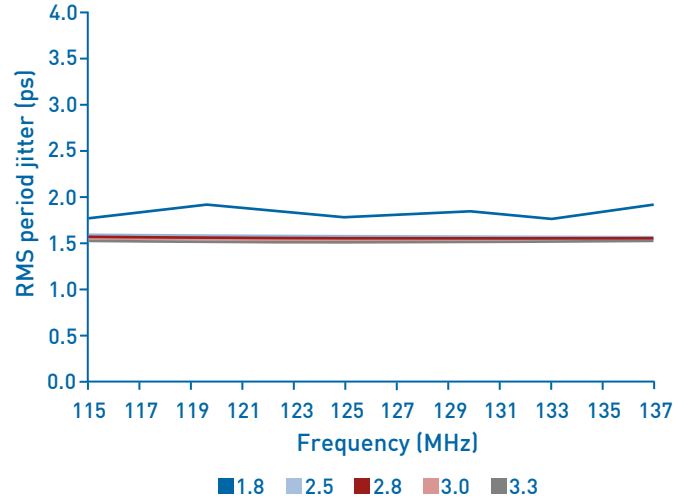


FIGURE 9. RMS PHASE JITTER vs. FREQUENCY

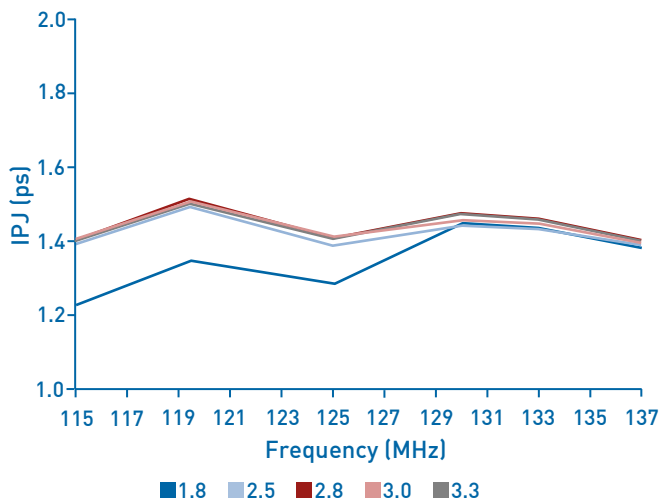


FIGURE 10. RMS PHASE JITTER vs. FREQUENCY

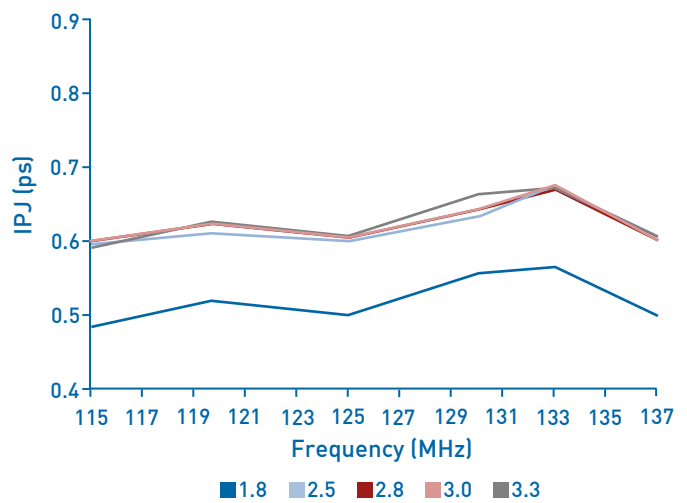


FIGURE 11. DUTY CYCLE vs. FREQUENCY

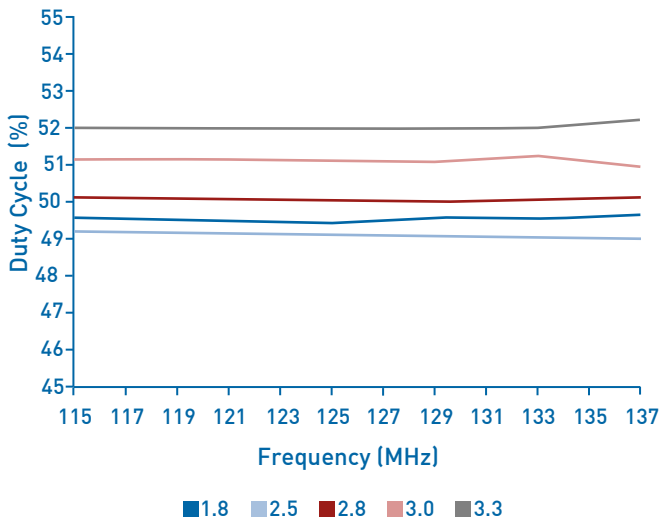
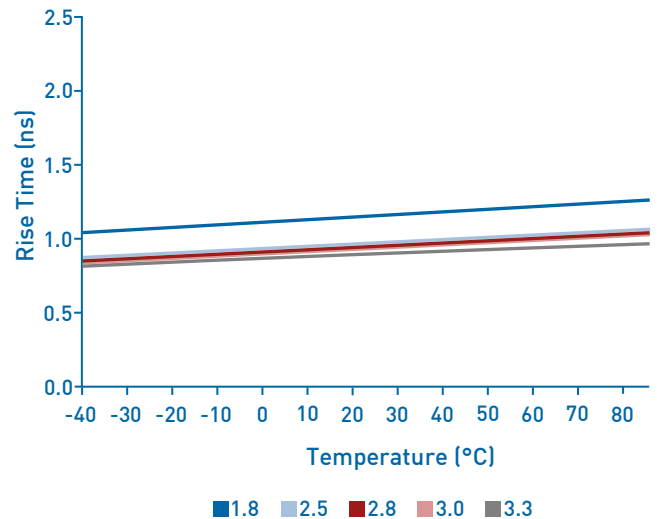


FIGURE 12. RISE TIME vs. TEMPERATURE, 125 MHz OUTPUT



Note: 5. All plots are measured with 15 pF load at room temperature, unless otherwise stated.

## PROGRAMMABLE DRIVE STRENGTH

The LPOP includes a programmable drive strength feature named SoftLevel to provide a simple, flexible tool to optimize the clock rise/fall time for specific applications. Benefits from the programmable drive strength feature are:

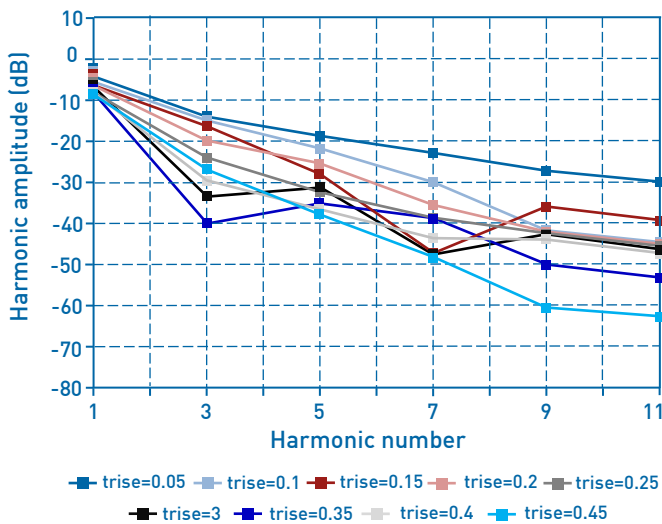
- + Improves system radiated electromagnetic interference (EMI) by slowing down the clock rise/fall time
- + Improves the downstream clock receiver's (RX) jitter by decreasing (speeding up) the clock rise/fall time.
- + Ability to drive large capacitive loads while maintaining full swing with sharp edge rates.

For more detailed information about rise/fall time control and drive strength selection, see the Petermann-Technik Applications Note section: <http://www.petermann-technik.com>

### EMI REDUCTION BY SLOWING RISE/FALL TIME (SoftLevel FUNCTION)

Figure 13 shows the harmonic power reduction as the rise/fall times are increased (slowed down). The rise/fall times are expressed as a ratio of the clock period. For the ratio of 0.05, the signal is very close to a square wave. For the ratio of 0.45, the rise/fall times are very close to near-triangular waveform. These results, for example, show that the 11th clock harmonic can be reduced by 35 dB if the rise/fall edge is increased from 5% of the period to 45% of the period.

FIGURE 13. HARMONIC EMI REDUCTION AS A FUNCTION OF SLOWER RISE/FALL TIME (SoftLevel FUNCTION)



### JITTER REDUCTION WITH FASTER RISE/FALL TIME

Power supply noise can be a source of jitter for the downstream chipset. One way to reduce this jitter is to increase rise/fall time (edge rate) of the input clock. Some chipsets would require faster rise/fall time in order to reduce their sensitivity to this type of jitter. The LPOP provides up to 3 additional high drive strength settings for very fast rise/fall time. Refer to the rise/fall time tables to determine the proper drive strength.

### HIGH OUTPUT LOAD CAPABILITY

The rise/fall time of the input clock varies as a function of the actual capacitive load the clock drives. At any given drive strength, the rise/fall time becomes slower as the output load increases. As an example, for a 3.3V LPOP device with default drive strength setting, the typical rise/fall time is 1ns for 15 pF output load. The typical rise/fall time slows down to 2.6 ns when the output load increases to 45 pF. One can choose to speed up the rise/fall time to 1.68 ns by then increasing the drive strength setting on the LPOP.

The LPOP can support up to 60 pF or higher in maximum capacitive loads with up to 3 additional drive strength settings. Refer to the Rise/Fall Time Tables to determine the proper drive strength for the desired combination of output load vs. rise/fall time.

### LPOP DRIVE STRENGTH SELECTION

Tables 1 through 5 define the rise/fall time for a given capacitive load and supply voltage.

1. Select the table that matches the LPOP nominal supply voltage (1.8V, 2.5V, 2.8V, 3.0V, 3.3V).
2. Select the capacitive load column that matches the application requirement (5 pF to 30 pF)
3. Under the capacitive load column, select the desired rise/fall times.
4. The left-most column represents the part number code for the corresponding drive strength.
5. Add the drive strength code to the part number for ordering purposes.

### CALCULATING MAXIMUM FREQUENCY

Based on the rise and fall time data given in Tables 1 through 5, the maximum frequency the oscillator can operate with guaranteed full swing of the output voltage over temperature as follows:

$$\text{Max. frequency} = \frac{1}{6 \times (\text{Trise})}$$

### EXAMPLE 1

Calculate  $f_{\text{MAX}}$  for the following condition:

- + VDD = 3.3V (Table 1)
- + Capacitive Load: 30pF
- + Desired Tr/tf time = 2ns (rise/fall time part number code=U)

Part number for the above example:

LPOP33-2520-E-25-M-125.000MHz-T-U



Drive strength code is inserted here. Standard setting is "S"

## RISE/FALL TIME (20% TO 80%) vs C<sub>LOAD</sub>

TABLE 1. VDD = 1.8V RISE/FALL TIMES FOR SPECIFIC C<sub>LOAD</sub>

RISE/FALL TIME TYP (NS)		
Drive Strength \ C <sub>LOAD</sub>	5 pF	15 pF
T	0.93	n/a <sup>(6)</sup>
E	0.78	n/a
U	0.70	1.48
S = standard limit	0.65	1.30

TABLE 2. VDD = 2.5V RISE/FALL TIMES FOR SPECIFIC C<sub>LOAD</sub>

RISE/FALL TIME TYP (NS)		
Drive Strength \ C <sub>LOAD</sub>	5 pF	15 pF
R	1.45	n/a
B	1.09	n/a
T	0.62	1.28
S = standard limit	0.54	1.00
U	0.43	0.96
F	0.34	0.88

TABLE 3. VDD = 2.8V RISE/FALL TIMES FOR SPECIFIC C<sub>LOAD</sub>

RISE/FALL TIME TYP (NS)			
Drive Strength \ C <sub>LOAD</sub>	5 pF	15 pF	30 pF
R	1.29	n/a	n/a
B	0.97	n/a	n/a
T	0.55	1.12	n/a
S = standard limit	0.44	1.00	n/a
U	0.34	0.88	n/a
F	0.29	0.81	1.48

TABLE 4. VDD = 3.0V RISE/FALL TIMES FOR SPECIFIC C<sub>LOAD</sub>

RISE/FALL TIME TYP (NS)			
Drive Strength \ C <sub>LOAD</sub>	5 pF	15 pF	30 pF
R	1.22	n/a	n/a
B	0.89	n/a	n/a
S = standard limit	0.51	1.00	n/a
E	0.38	0.92	n/a
U	0.30	0.83	n/a
F	0.27	0.76	1.39

TABLE 5. VDD = 3.3V RISE/FALL TIMES FOR SPECIFIC C<sub>LOAD</sub>

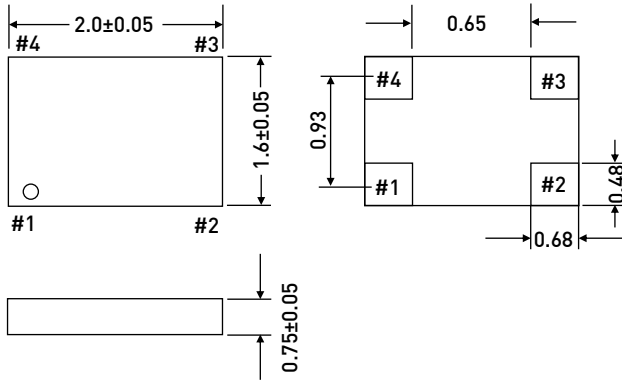
RISE/FALL TIME TYP (NS)			
Drive Strength \ C <sub>LOAD</sub>	5 pF	15 pF	30 pF
R	1.16	n/a	n/a
B	0.81	n/a	n/a
S = standard limit	0.46	1.00	n/a
E	0.33	0.87	n/a
U	0.28	0.79	1.46
F	0.25	0.72	1.31

Note: 6. "n/a" indicates that the resulting rise/fall time from the respective combination of the drive strength and output load does not provide rail-to-rail swing and is not available

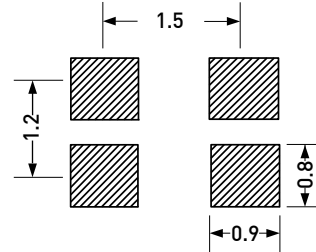
## DIMENSIONS AND PATTERNS

### PACKAGE SIZE - DIMENSIONS (UNIT:MM)

2.0 X 1.6 X 0.75 MM

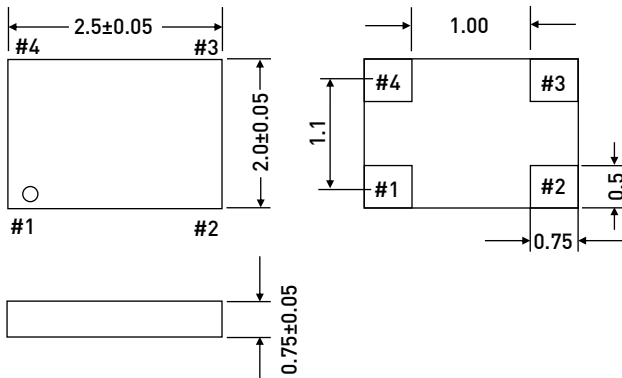


### RECOMMENDED LAND PATTERN (UNIT:MM)<sup>[7]</sup>

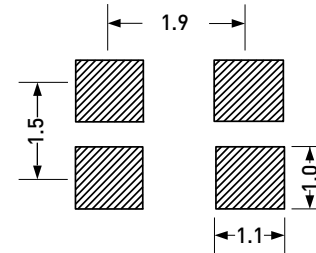


### PACKAGE SIZE - DIMENSIONS (UNIT:MM)

2.5 X 2.0 X 0.75 MM

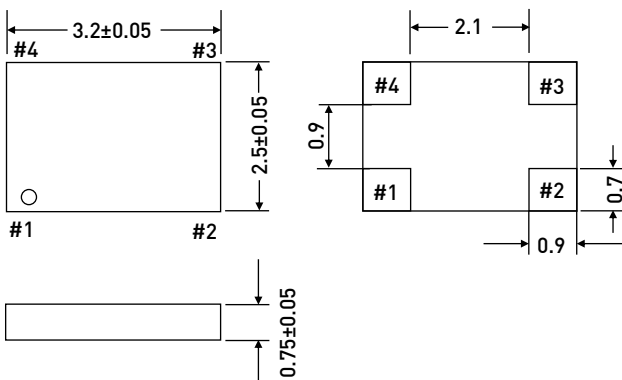


### RECOMMENDED LAND PATTERN (UNIT:MM)

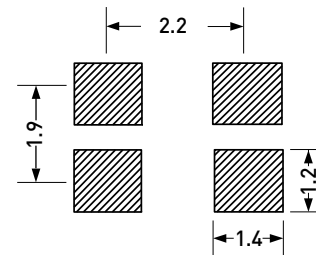


### PACKAGE SIZE - DIMENSIONS (UNIT:MM)

3.2 X 2.5 X 0.75 MM



### RECOMMENDED LAND PATTERN (UNIT:MM)

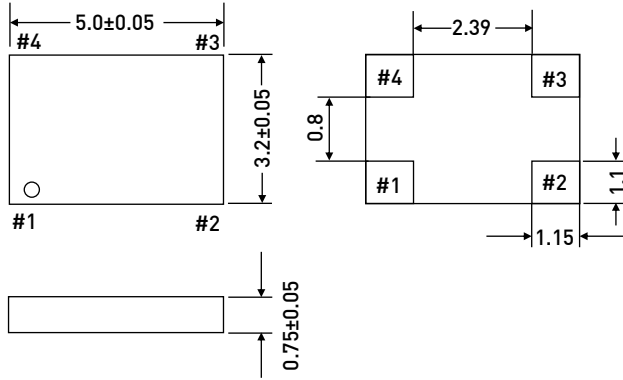


Note: 7. A capacitor value of 0.1  $\mu$ F between  $V_{DD}$  and GND is recommended (see note 2 + 3).

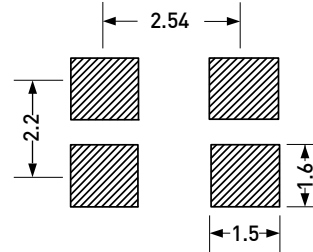
## DIMENSIONS AND PATTERNS

### PACKAGE SIZE - DIMENSIONS (UNIT:MM)

5.0 X 3.2 X 0.75 MM

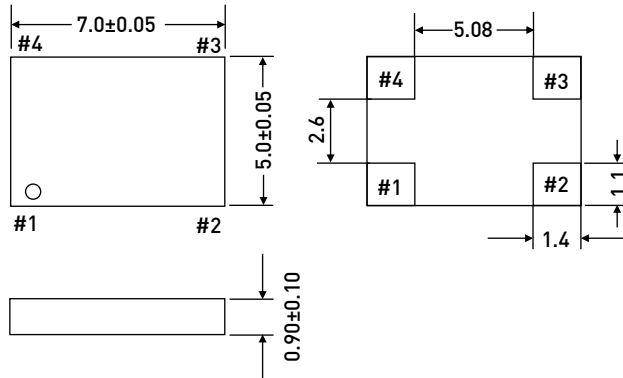


### RECOMMENDED LAND PATTERN (UNIT:MM)<sup>[8]</sup>

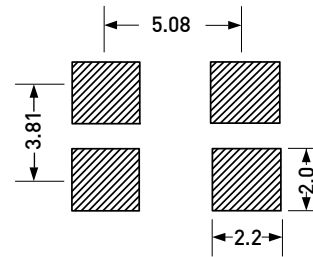


### PACKAGE SIZE - DIMENSIONS (UNIT:MM)

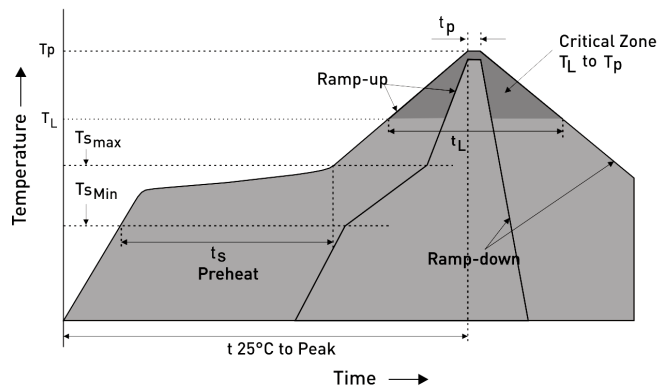
7.0 X 5.0 X 0.90 MM



### RECOMMENDED LAND PATTERN (UNIT:MM)



### REFLOW SOLDER PROFILE

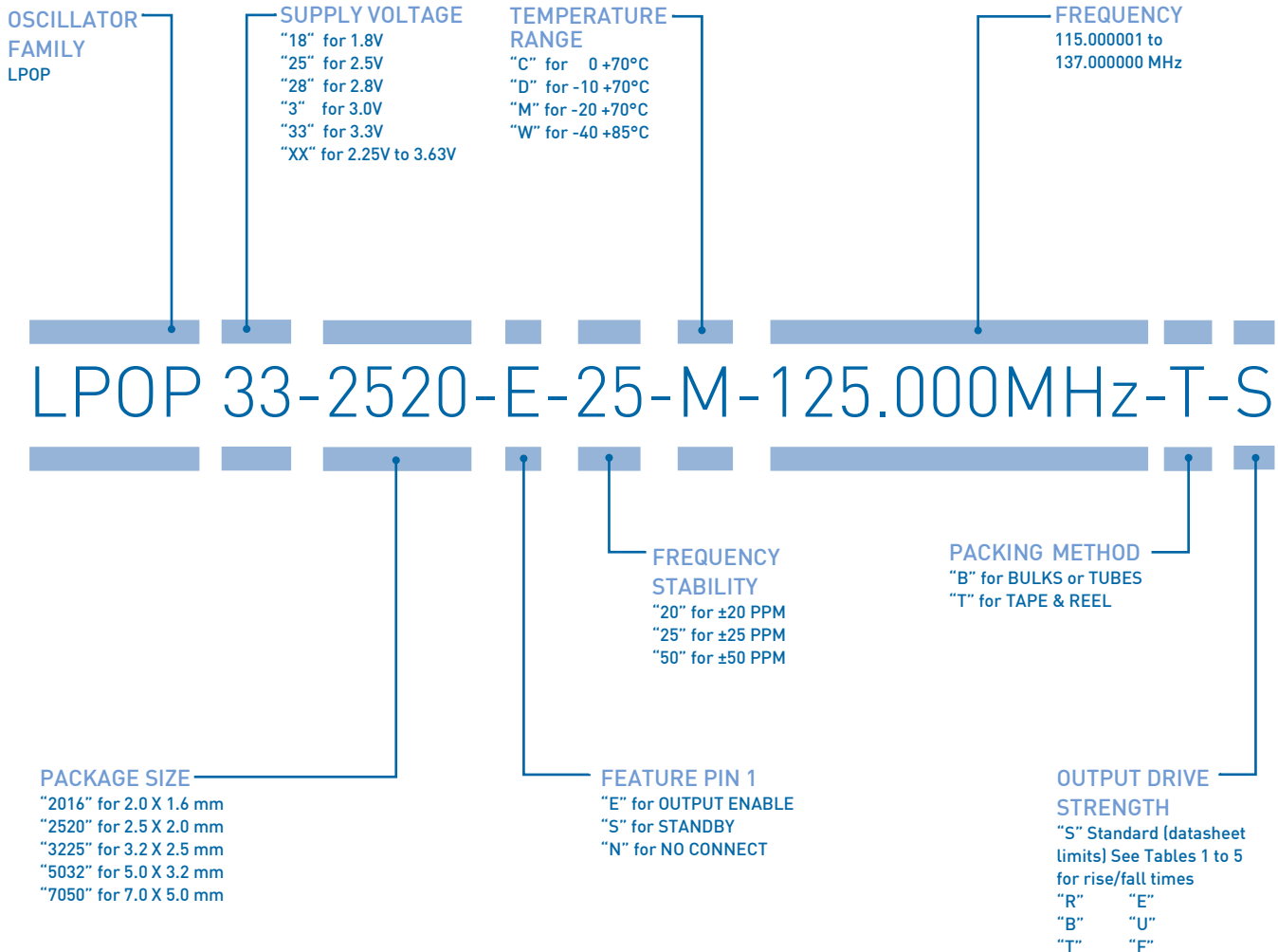


IPC/JEDEC Standard	IPC/JEDEC J-STD-020
Moisture Sensitivity Level	Level 1
TS MAX to TL (Ramp-up Rate)	3°C/second Maximum
Preheat	
- Temperature Minimum (TS MIN)	150°C
- Temperature Typical (TS TYP)	175°C
- Temperature Typical (TS MAX)	200°C
- Time (tS)	60 - 180 Seconds
Ramp-up Rate (TL to TP)	3°C/second Maximum
Time Maintained Above:	
- Temperature (TL)	217°C
- Time (TL)	60 - 150 Seconds
Peak Temperature (TP)	260°C Maximum
Target Peak Temperature (TP Target)	255°C
Time within 5°C of actual peak (tP)	20 - 40 Seconds
Max. Number of Reflow Cycles	3
Ramp-down Rate	6°C/second Maximum
Time 25°C to Peak Temperature (t)	8 minutes Maximum

Note: 8. A capacitor value of 0.1  $\mu$ F between  $V_{DD}$  and GND is recommended (see note 2 + 3).



## ORDERING INFORMATION



EXAMPLE: LPOP33-2520-E-25-M-125.000MHz-T-S

[PLEASE CLICK HERE TO CREATE YOUR OWN ORDERING CODE](#)

**EXPRESS SAMPLES ARE DELIVERABLE ON THE SAME DAY IF ORDERED UNTIL 02:00 PM!**



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